Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1-20. (canceled)

21. (currently amended) A wafer level chip scale package comprising;

a semiconductor die having a plurality of pads on a surface;

conductors coupled to and extending vertically a first predetermined distance from ~~the~~ said surface of ~~the~~ said semiconductor die;

an etch resistant layer on free ends of ~~the~~ said vertical conductors;

a layer of insulation on ~~the~~ said surface, ~~the~~ said layer of insulation having an exposed surface a second predetermined distance from ~~the~~ said surface of ~~the~~ said semiconductor die, wherein ~~the~~ said second predetermined distance is less than ~~the~~ said first predetermined distance and wherein said layer of insulation partially covers lower portions of side surfaces of substantially all of said conductors; and

reflowable material attached to ~~the~~ said etch resistant layer and to at least portions of side surfaces not covered by said layer of insulation of substantially all of ~~the~~ said conductors.

22. (original) A wafer level chip scale package in accordance with claim 21 wherein the conductors comprise copper conductors.

23. (original) A wafer level chip scale package in accordance with claim 22 wherein each of the copper conductors comprise a plurality of plated copper layers.

24. (original) A wafer level chip scale package in accordance with claim 21 wherein the etch resistant layer comprises a layer of gold.

25. (original) A wafer level chip scale package in accordance with claim 21 wherein the etch resistant layer comprises a layer of nickel with a layer of gold thereon.

26. (original) A wafer level chip scale package in accordance with claim 25 wherein the thickness of the layer of gold is less than the difference between the first predetermined distance and the second predetermined distance.

27. (original) A wafer level chip scale package in accordance with claim 21 wherein the layer of insulation comprises a material selected from the group including mold compound, encapsulant epoxy, underfill coating, and photo imageable material, such as benzocyclobutene (BCB) or polyimide.

28. (original) A wafer level chip scale package in accordance with claim 21 wherein the reflowable material comprises solder.

29. (original) A wafer level chip scale package in accordance with claim 28 wherein the solder comprises eutectic solder.

30-49. (canceled)

50-58. (canceled)